Kodak

DEVICE
PERFORMANCE
SPECIFICATION

KODAK KAI-2001
KODAK KAI-2001M
KODAK KAI-2001CM
Image Sensor

1600 (H) x 1200 (V)
Interline Transfer
Progressive Scan CCD

June 16 2003
Revision 1.0

www.kodak.com/go/imagers 585-722-4385 Email: imagers@kodak.com

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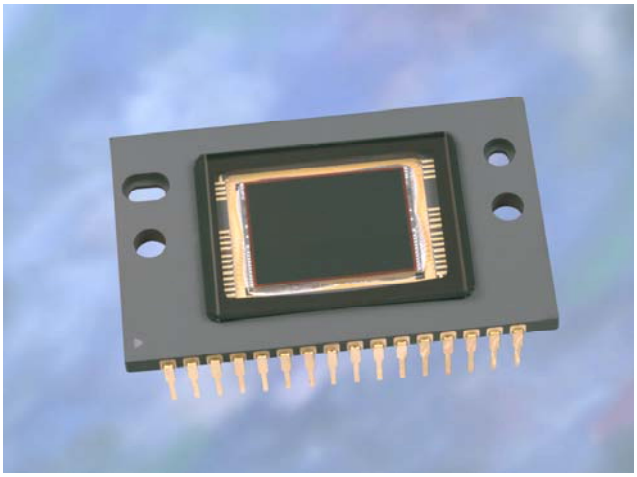
SUMMARY SPECIFICATION

KODAK KAI-2001 Image Sensor 1600 (H) x 1200 (V) Interline Transfer Progressive Scan CCD



Description

The Kodak KAI-2001 Image Sensor is a high-performance 2-million pixel sensor designed for a wide range of medical, scientific and machine vision applications. The 7.4µm square pixels with microlenses provide high sensitivity and the large full well capacity results in high dynamic range. The split horizontal register offers a choice of single or dual output allowing either 15 or 30 frame per second (fps) video rate for the progressively scanned images. Also included is a fast line dump for sub-sampling at higher frame rates. The vertical overflow drain structure provides antiblooming protection and enables electronic shuttering for precise exposure control. Other features include low dark current, negligible lag and low smear.

Parameter	Value
Architecture	Interline CCD; Progressive Scan
Total Number of Pixels	1640 (H) x 1214 (V) = approx. 1.99M
Number of Effective Pixels	1608 (H) x 1208 (V) = approx. 1.94M
Number of Active Pixels	1600 (H) x 1200 (V) = approx. 1.92M
Number of Outputs	1 or 2
Pixel Size	7.4µm (H) x 7.4µm (V)
Imager Size	14.803mm (diagonal)
Chip Size	13.38mm (H) x 9.52mm (V)
Aspect Ratio	4:3
Saturation Signal	40,000 e
Peak Quantum Efficiency (KAI-2001M)	55%
Peak Quantum Efficiency (KAI-2001CM) RGB	45%, 42%, 35%
Output Sensitivity	16 µV/e
Total System Noise (at 40MHZ)	40 e
Total System Noise (at 20MHz)	23 e
Dark Current	< 0.5 nA/cm2
Dark Current Doubling Temperature	7°C
Dynamic Range	60 dB
Charge Transfer Efficiency	> 0.99999
Blooming Suppression	300X
Smear	80 dB
Image Lag	<10 e
Maximum Data Rate	40 MHz

All parameters above are specified at T = 40*C

REVISION NO.: 1.0
EFFECTIVE DATE: June 16, 2003

DEVICE DESCRIPTION

Architecture

Overall

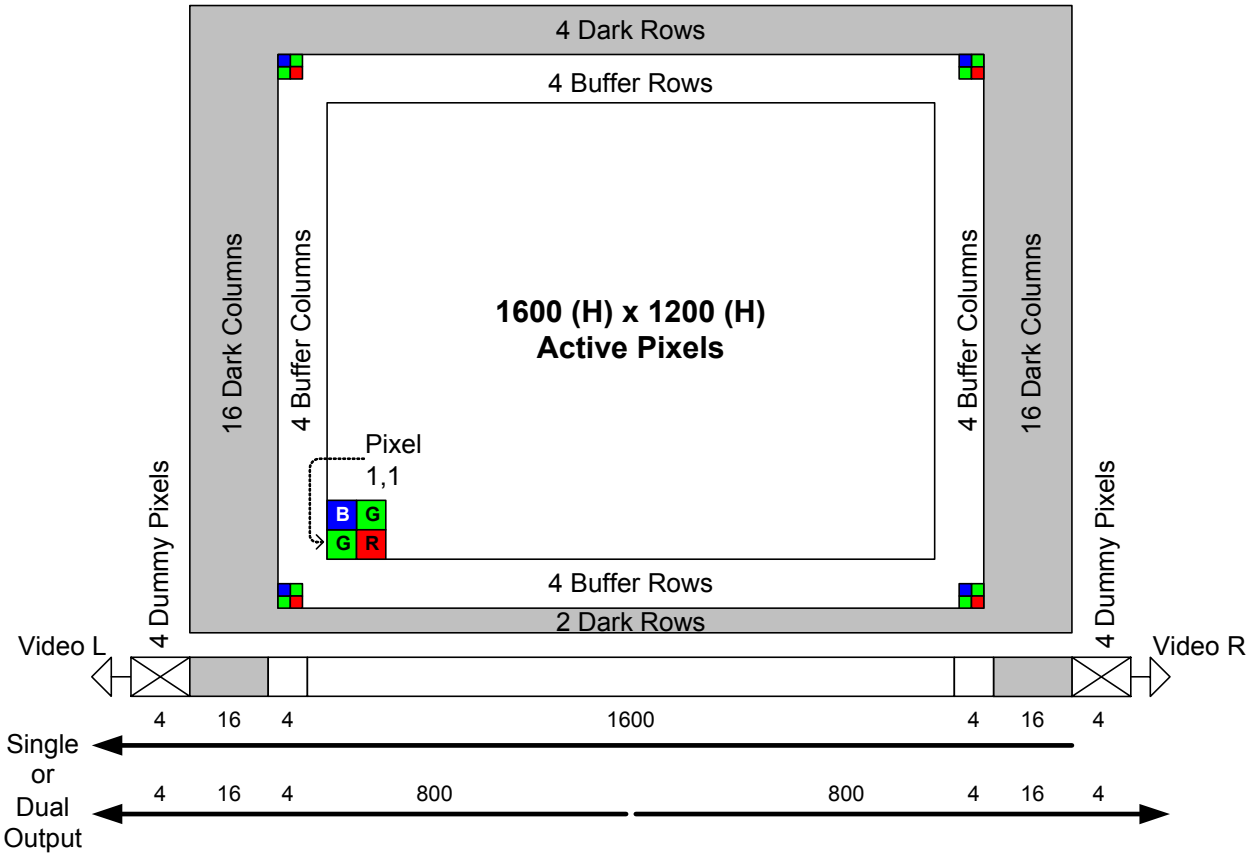


Figure 1 - Sensor Architecture

There are 2 light shielded rows followed 1208 photoactive rows and finally 4 more light shielded rows. The first 4 and the last 4 photoactive rows are buffer rows giving a total of 1200 lines of image data.

In the single output mode all pixels are clocked out of the Video L output in the lower left corner of the sensor. The first 4 empty pixels of each line do not receive charge from the vertical shift register. The next 16 pixels receive charge from the left light shielded edge followed by 1608 photosensitive pixels and finally 16 more light shielded pixels from the right edge of the sensor. The first and last 4 photosensitive pixels are buffer pixels giving a total of 1600 pixels of image data.

In the dual output mode the clocking of the right half of the horizontal CCD is reversed. The left half of the image is clocked out Video L and the right half of the image is clocked out Video R. Each row consists of 4 empty pixels followed by 16 light shielded pixels followed by 800 photosensitive pixels. When reconstructing the image, data from Video R will have to be reversed in a line buffer and appended to the Video L data.

Pixel

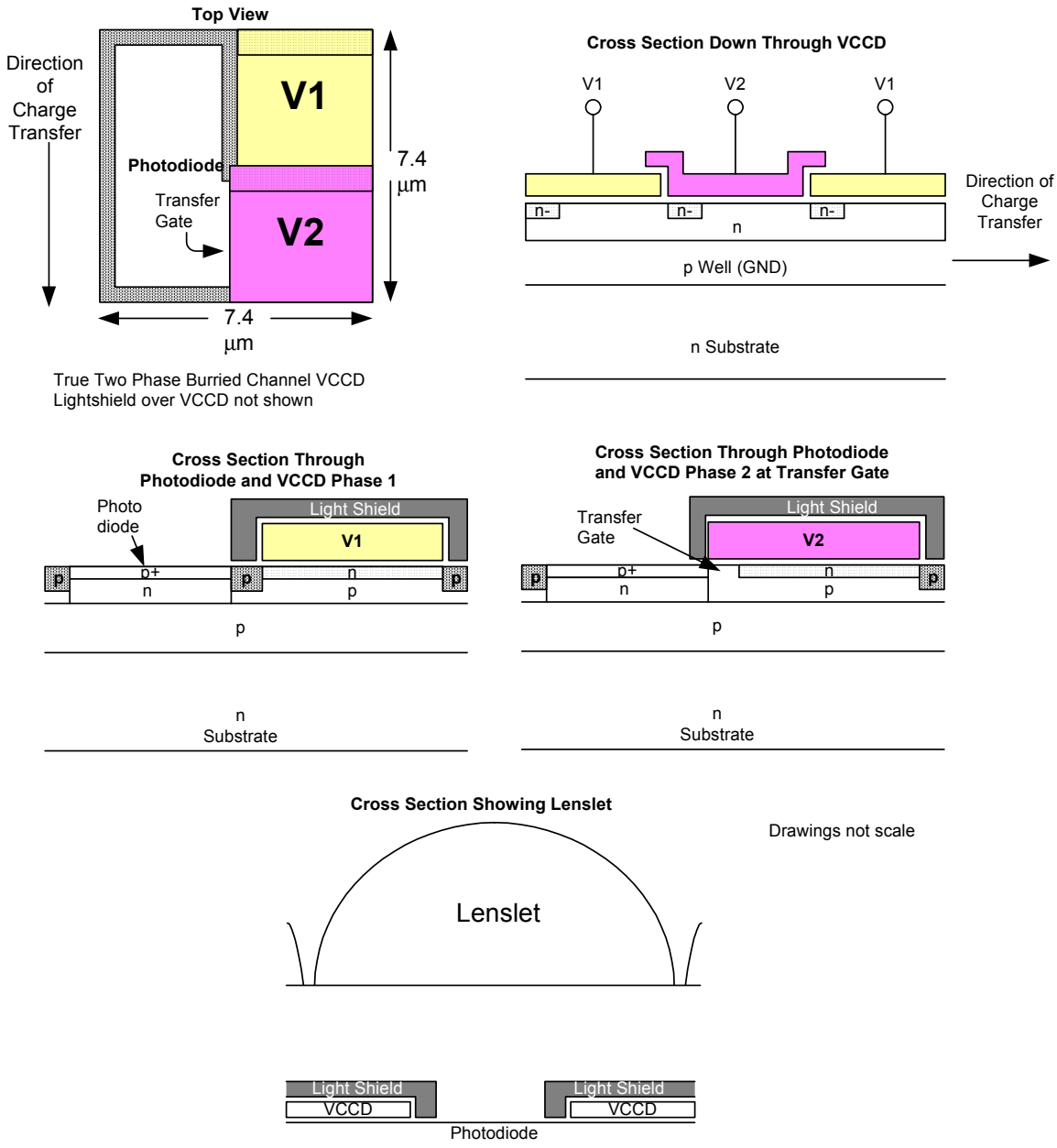


Figure 2 - Pixel Architecture

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependant upon light level and exposure time and non-linearly dependant on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

Vertical to Horizontal Transfer

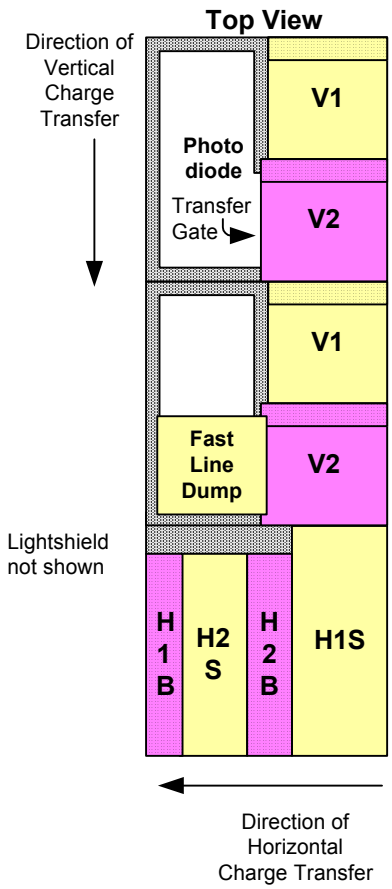


Figure 3 - Vertical to Horizontal Transfer Architecture

When the V1 and V2 timing inputs are pulsed, charge in every pixel of the VCCD is shifted one row towards the HCCD. The last row next to the HCCD is shifted into the HCCD. When the VCCD is shifted, the timing signals to the HCCD must be stopped. H1 must be stopped in the high state and H2 must be stopped in the low state. The HCCD clocking may begin THD µs after the falling edge of the V1 and V2 pulse.

Charge is transferred from the last vertical CCD phase into the H1S horizontal CCD phase. Refer to Figure 23 for an example of timing that accomplishes the vertical to horizontal transfer of charge.

If the fast line dump is held at the high level (FDH) during a vertical to horizontal transfer, then the entire line is removed and not transferred into the horizontal register.

Horizontal Register to Floating Diffusion

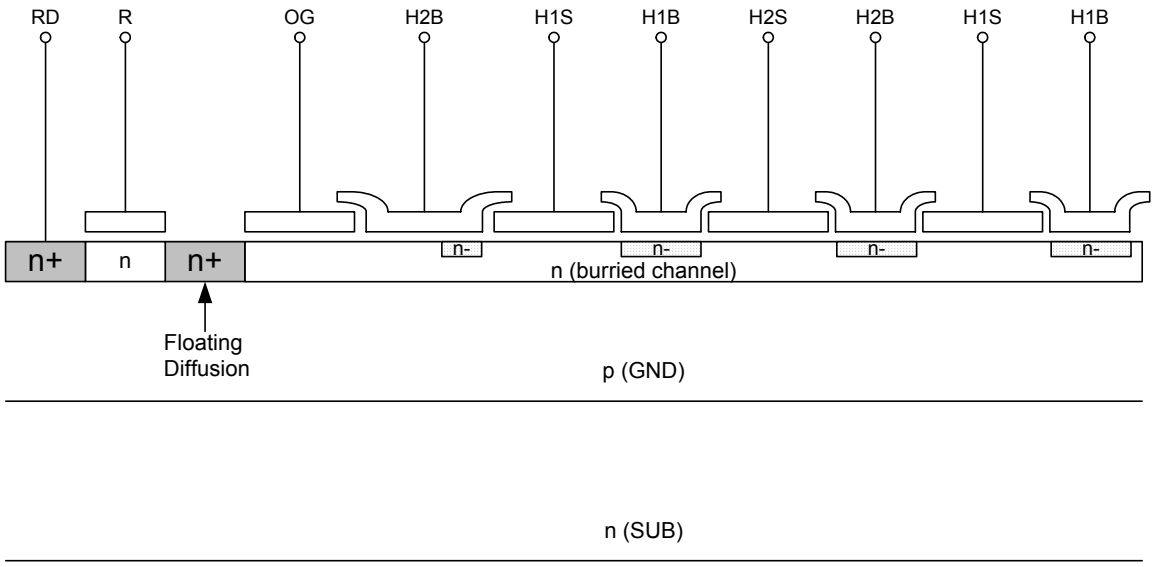


Figure 4 - Horizontal Register to Floating Diffusion Architecture

The HCCD has a total of 1648 pixels. The 1640 vertical shift registers (columns) are shifted into the center 1640 pixels of the HCCD. There are 4 pixels at both ends of the HCCD, which receive no charge from a vertical shift register. The first 4 clock cycles of the HCCD will be empty pixels (containing no electrons). The next 16 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. The next 1608 clock cycles will contain photo-electrons (image data). Finally, the last 16 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. Of the 16 dark columns, the first and last dark columns should not be used for determining the zero signal level. Some light does leak into the first and last dark columns. Only use the center 14 columns of the 16 column dark reference.

When the HCCD is shifting valid image data, the timing inputs to the electronic shutter (SUB), VCCD (V1, V2), and fast line dump (FD) should be not be pulsed. This prevents unwanted noise from being introduced. The HCCD is a type of charge coupled device known as a pseudo-two phase CCD. This type of CCD has the ability to shift charge in two directions. This allows the entire image to be shifted out to the video L output, or to the video R output (left/right image reversal). The HCCD is split into two equal halves of 824 pixels each. When operating the sensor in single output mode the two halves of the HCCD are shifted in the same direction. When operating the sensor in dual output mode the two halves of the HCCD are shifted in opposite directions. The direction of charge transfer in each half is controlled by the H1BL, H2BL, H1BR, and H2BR timing inputs.

Horizontal Register Split

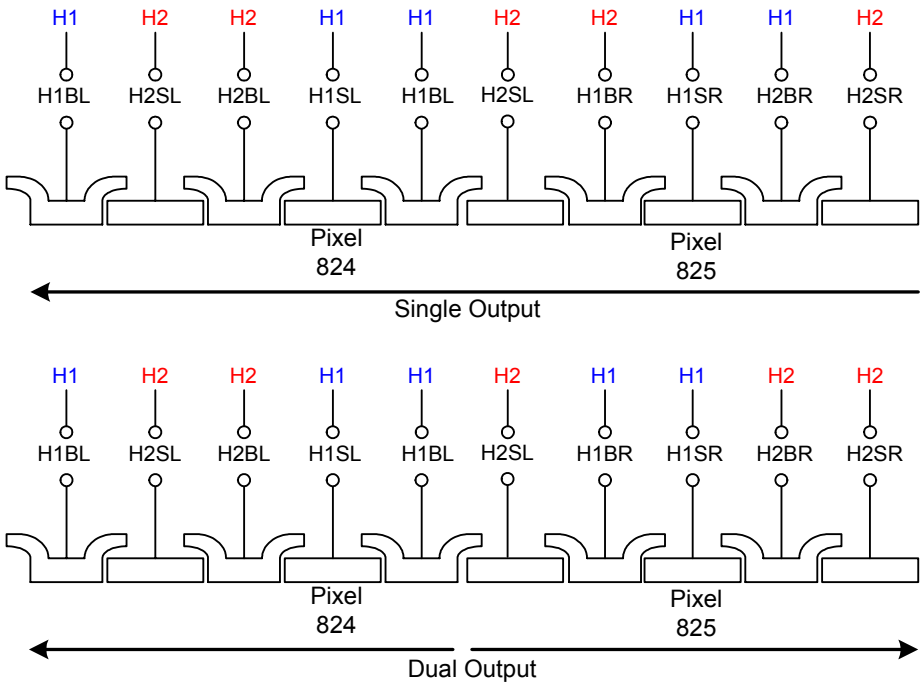


Figure 5 - Horizontal Register

Single Output Operation

When operating the sensor in single output mode all pixels of the image sensor will be shifted out the Video L output (pin 31). To conserve power and lower heat generation the output amplifier for Video R may be turned off by connecting VDDR (pin 24) and VOUTR (pin 24) to GND (zero volts).

The H1 timing from the timing diagrams should be applied to H1SL, H1BL, H1SR, H2BR, and the H2 timing should be applied to H2SL, H2BL, H2SR, and H1BR. In other words, the clock driver generating the H1 timing should be connected to pins 4, 3, 13, and 15. The clock driver generating the H2 timing should be connected to pins 5, 2, 12, and 14. The horizontal CCD should be clocked for 4 empty pixels plus 16 light shielded pixels plus 1608 photoactive pixels plus 16 light shielded pixels for a total of 1644 pixels.

Dual Output Operation

In dual output mode the connections to the H1BR and H2BR pins are swapped from the single output mode to change the direction of charge transfer of the right side horizontal shift register. In dual output mode both VDDL and VDDR (pins 25, 24) should be connected to 15V. The H1 timing from the timing diagrams should be applied to H1SL, H1BL, H1SR, H1BR, and the H2 timing should be applied to H2SL, H2BL, H2SR, and H2BR. The clock driver generating the H1 timing should be connected to pins 4, 3, 13, and 14. The clock driver generating the H2 timing should be connected to pins 5, 2, 12, and 15. The horizontal CCD should be clocked for 4 empty pixels plus 16 light shielded pixels plus 804 photoactive pixels for a total of 824 pixels. If the camera is to have the option of dual or single output mode, the clock driver signals sent to H1BR and H2BR may be swapped by using a relay. Another alternative is to have two extra clock drivers for H1BR and H2BR and invert the signals in the timing logic generator. If two extra clock drivers are used, care must be taken to ensure the rising and falling edges of the H1BR and H2BR clocks occur at the same time (within 3ns) as the other HCCD clocks.

Output

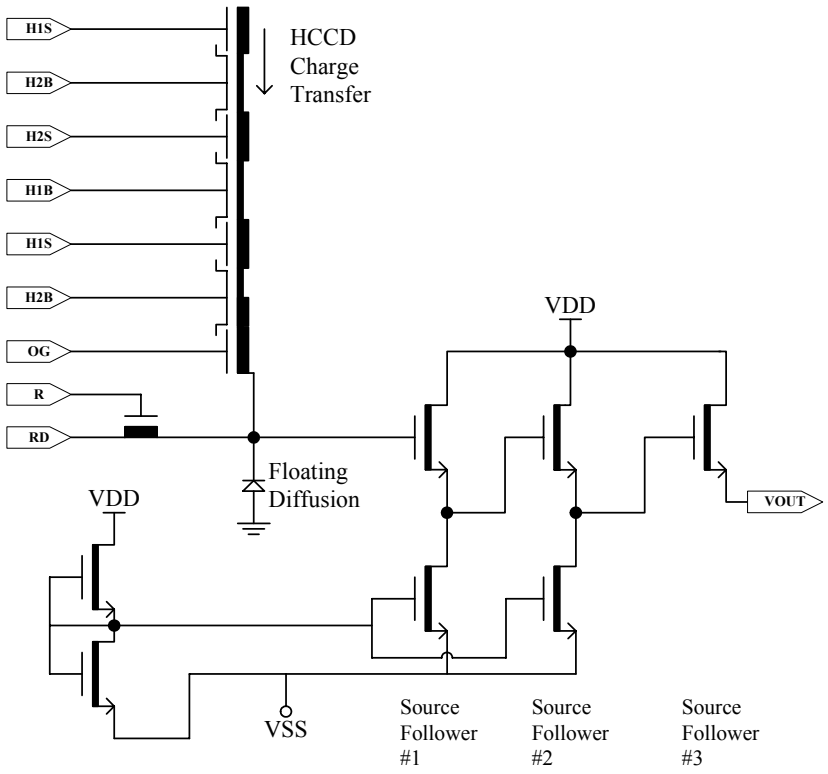


Figure 6 - Output Architecture

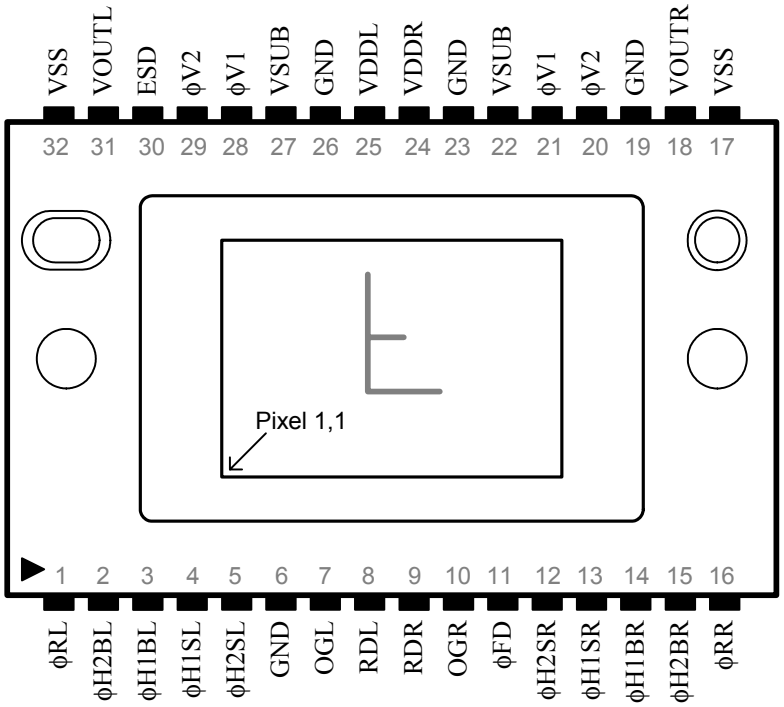
Charge packets contained in the horizontal register are dumped pixel by pixel onto the floating diffusion (fd) output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential charge is determined by the expression $\Delta Vfd=\Delta Q/Cfd$. A three-stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain. The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of microvolts per electron ($\mu V/e^-$). After the signal has been sampled off chip, the reset clock (R) removes the charge from the floating diffusion and resets its potential to the reset drain voltage (RD).

When the image sensor is operated in the binned or summed interlaced modes there will be more than 40,000 electrons in the output signal. The image sensor is designed with a 16µV/e charge to voltage conversion on the output. This means a full signal of 40,000 electrons will produce a 640mV change on the output amplifier. The output amplifier was designed to handle an output swing of 640mV at a pixel rate of 40MHz. If 80,000 electron charge packets are generated in the binned or summed interlaced modes then the output amplifier output will have to swing 1280mV. The output amplifier does not have enough bandwidth (slew rate) to handle 1280mV at 40MHz. Hence, the pixel rate will have to be reduced to 20MHz if the full dynamic range of 80,000 electrons is desired.

The charge handling capacity of the output amplifier is also set by the reset clock voltage levels. The reset clock driver circuit is very simple if an amplitude of 5V is used. But the 5V amplitude restricts the output amplifier charge capacity to 40,000 electrons. If the full dynamic range of 80,000 electrons is desired then the reset clock amplitude will have to be increased to 7V.
If you only want a maximum signal of 40,000 electrons in binned or summed interlaced modes, then a 40 MHz pixel rate with a 5V reset clock may be used. The output of the amplifier will be unpredictable above 40,000 electrons so be sure to set the maximum input signal level of your analog to digital converter to the equivalent of 40,000 electrons (640mV).

Physical Description

Pin Description and Device Orientation



Pin	Name	Description	Pin	Name	Description
1	φRL	Reset Gate, Left	32	VSS	Output Amplifier Return
2	φH2BL	H2 Barrier, Left	31	VOUTL	Video Output, Left
3	φH1BL	H1 Barrier, Left	30	ESD	ESD
4	φH1SL	H1 Storage, Left	29	φV2	Vertical Clock, Phase 2
5	φH2SL	H2 Storage, Left	28	φV1	Vertical Clock, Phase 1
6	GND	Ground	27	VSUB	Substrate
7	OGL	Output Gate, Left	26	GND	Ground
8	RDL	Reset Drain, Left	25	VDDL	Vdd, Left
9	RDR	Reset Drain, Right	24	VDDR	Vdd, Right
10	OGR	Output Gate, Right	23	GND	Ground
11	FD	Fast Line Dump Gate	22	VSUB	Substrate
12	φH2SR	H2 Storage, Right	21	φV1	Vertical Clock, Phase 1
13	φH1SR	H1 Storage, Right	20	φV2	Vertical Clock, Phase 2
14	φH1BR	H1 Barrier, Right	19	GND	Ground
15	φH2BR	H2 Barrier, Right	18	VOUTR	Video Output, Right
16	φRR	Reset Gate, Right	17	VSS	Output Amplifier Return

The pins are on a 0.07” spacing

PERFORMANCE

Power - Estimated

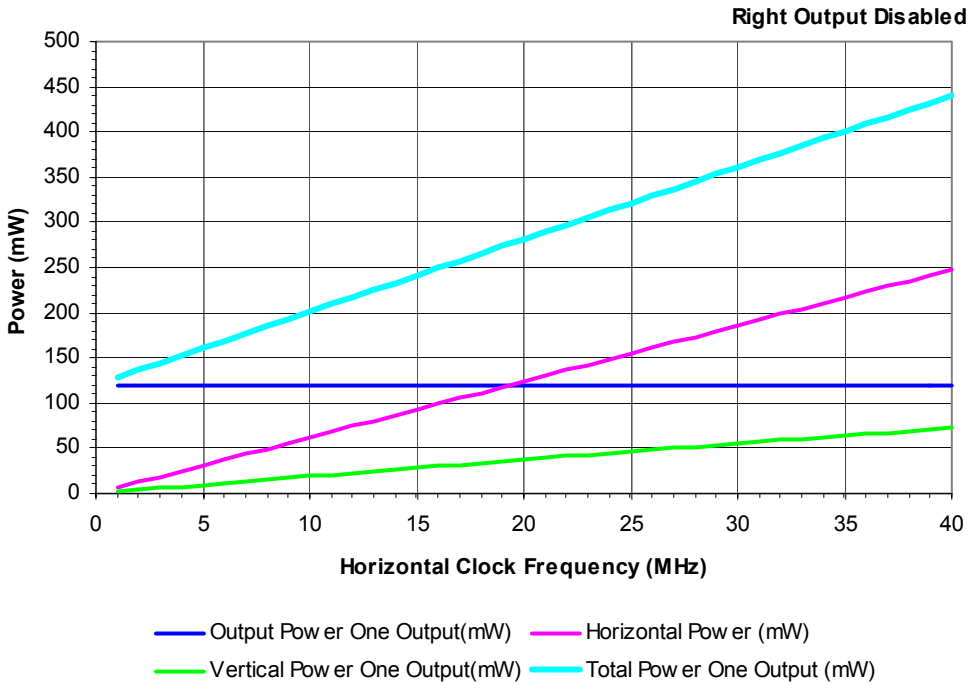


Figure 7 - Power

Frame Rates

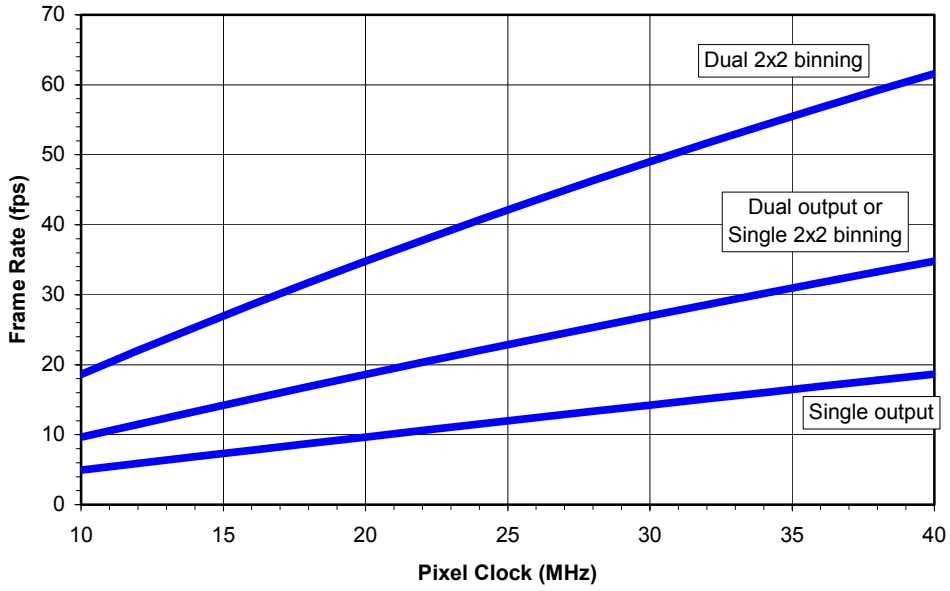


Figure 8 - Frame Rates

Imaging Performance

Image Performance Operational Conditions

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions:

Description	Condition	Notes
Frame time	237 msec	1
Horizontal clock frequency	10 MHz	
Light Source (LED)	Continuous red, green and blue illumination centered at 450, 530 and 650 nm	2,3
Operation	Nominal operating voltages and timing	

Notes:
1. Electronic shutter is not used. Integration time equals frame time.
2. LEDs used: Blue: Nichia NLPB500, Green: Nichia NSPG500S and Red: HP HLMP-8115.
3. For monochrome sensor, only green LED used.

Imaging Performance Specifications

KAI-2001M and KAI-2001CM

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature(s) Tested At (°C)	Notes	Test
Dark Center Uniformity		n/a	n/a	20	e^-rms	Die	27, 40		1
Dark Global Uniformity		n/a	n/a	5.0	mVpp	Die	27, 40		2
Global Uniformity		n/a	2.5	5.0	%rms	Die	27, 40	1	3
Global Peak to Peak Uniformity	PRNU	n/a	10	20	%pp	Die	27, 40	1	4
Center Uniformity		n/a	1.0	2.0	%rms	Die	27, 40	1	5
Maximum Photoresponse Nonlinearity	NL	n/a	2		%	Design		2,3	
Maximum Gain Difference Between Outputs	ΔG	n/a	10		%	Design		2,3	
Max. Signal Error due to Nonlinearity Dif.	ΔNL	n/a	1		%	Design		2,3	

Description (cont)	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature(s) Tested At (°C)	Notes	Test
Horizontal CCD Charge Capacity	Hne	n/a	100	n/a	ke^-	Design			
Vertical CCD Charge Capacity	VNe	n/a	50	n/a	ke^-	Die			
Photodiode Charge Capacity	PNe	38	40	n/a	ke^-	Die			
Horizontal CCD Charge Transfer Efficiency	HCTE	0.99999	n/a	n/a		Design			
Vertical CCD Charge Transfer Efficiency	VCTE	0.99999	n/a	n/a		Design			
Photodiode Dark Current	Ipd	n/a	40	350	e/p/s	Die			
Photodiode Dark Current	Ipd	n/a	0.01	0.1	nA/cm^2	Die			
Vertical CCD Dark Current	Ivd	n/a	400	1711	e/p/s	Die			
Vertical CCD Dark Current	Ivd	n/a	0.12	0.5	nA/cm^2	Die			
Image Lag	Lag	n/a	<10	50	e^-	Design			
Antiblooming Factor	Xab	100	300	n/a		Design			
Vertical Smear	Smr	n/a	80	75	DB	Design			
Total Noise	n_{e-T}		23		e^-rms	Design		5	
Total Noise	n_{e-T}		40		e^-rms	Design		6	
Dynamic Range	DR		60		dB	Design		6,7	
Output Amplifier DC Offset	V_{odc}	4	8.5	14	V	Die			
Output Amplifier Bandwidth	F_{-3db}		140		MHz	Design			
Output Amplifier Impedance	R_{OUT}	100	130	200	Ohms	Die			
Output Amplifier Sensitivity	$\Delta V/\Delta N$		16		$\mu V/e^-$	Design			

KAI-2001M

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature(s) Tested At (°C)	Notes	Test
Peak Quantum Efficiency	QE_{max}	45	55	n/a	%	Design			
Peak Quantum Efficiency Wavelength	λQE	n/a	500	n/a	nm	Design			

KAI-2001CM

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature(s) Tested At (°C)	Notes	Test
Peak Quantum Efficiency Red Green Blue	QE_{max}		45 42 35	n/a	%	Design			
Peak Quantum Efficiency Blue Wavelength Red Green	λQE	n/a	470 540 620	n/a	nm	Design			

n/a : not applicable

Notes:
1. For KAI-2001CM, per color
2. Value is over the range of 10% to 90% of photodiode saturation.
3. Value is for the sensor operated without binning
4. Includes system electronics noise, dark pattern noise and dark current shot noise at 20 MHz.
5. Includes system electronics noise, dark pattern noise and dark current shot noise at 40 MHz.
6. Uses 20LOG(PNe/ n_{e-T})

Defect Definitions

Description	Definition	Maximum	Temperature(s) tested at (°C)	Notes	Test
Major dark field defective pixel	Defect >= 179 mV	20	27, 40	1	
Major bright field defective pixel	Defect >= 15 %			1	
Minor dark field defective pixel	Defect >= 57 mV	200	27, 40		
Cluster defect	A group of 2 to 10 contiguous major defective pixels, but no more than 2 adjacent defects horizontally	8	27, 40	1	
Column defect	A group of more than 10 contiguous major defective pixels along a single column	0	27,40	1	

Notes:

1. There will be at least two non-defective pixels separating any two major defective pixels.

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point defects are not included in the defect map. All pixels are referenced to pixel 1,1 in the defect map.

Quantum Efficiency

Monochrome Quantum Efficiency

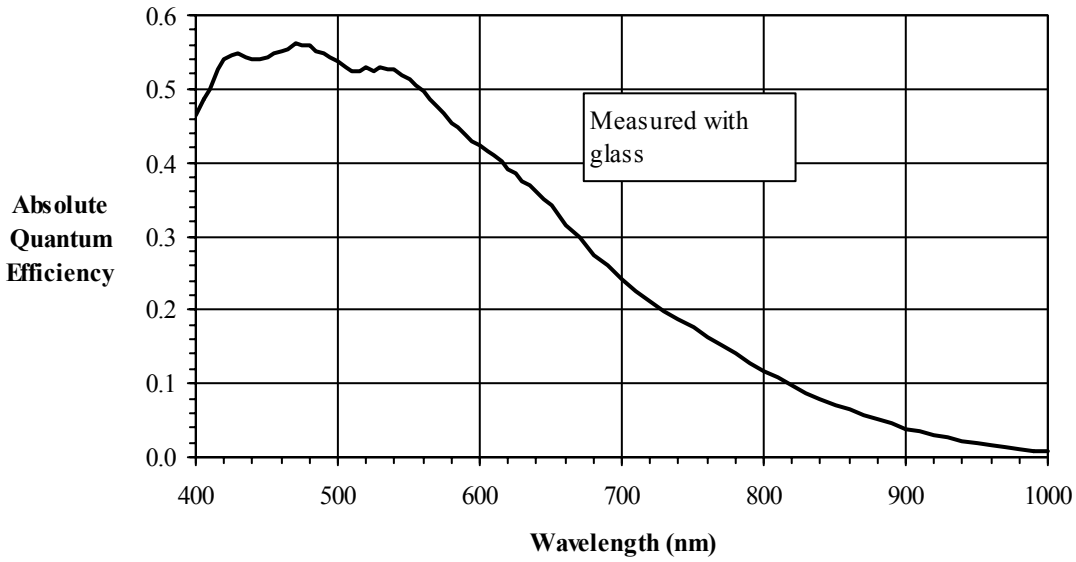


Figure 9 - Monochrome Quantum Efficiency

Color Quantum Efficiency

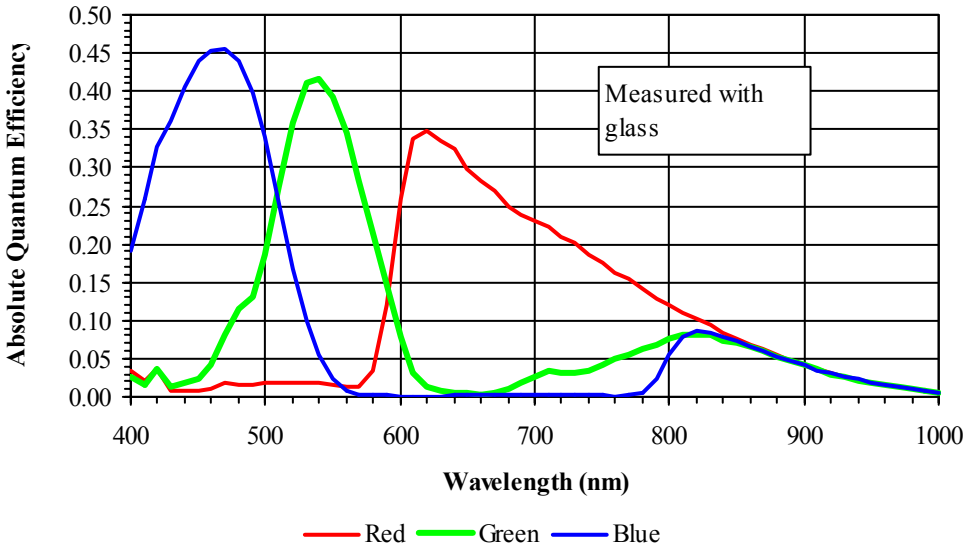


Figure 10 - Color Quantum Efficiency

Ultraviolet (UV) Quantum Efficiency

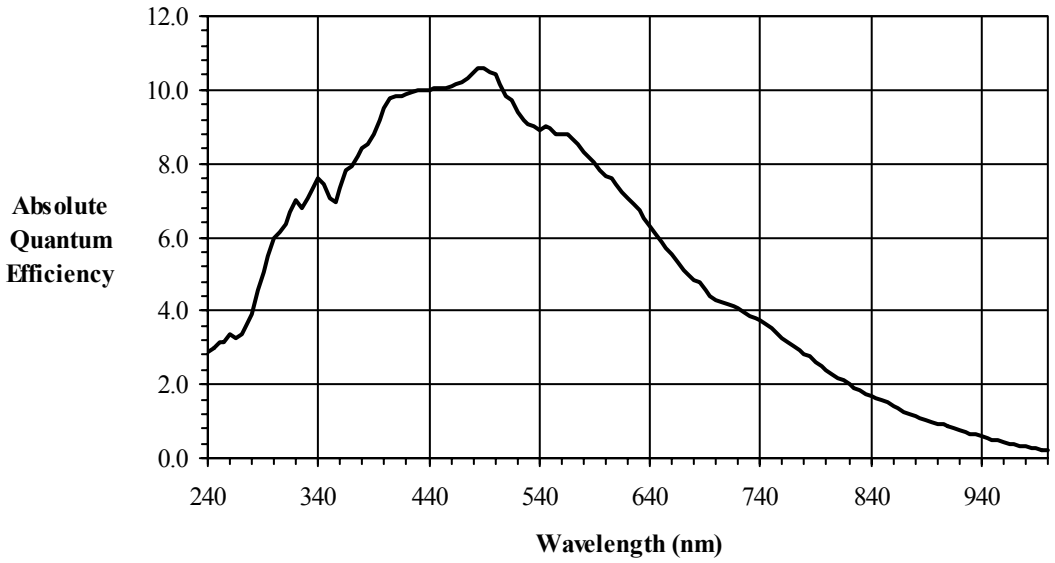


Figure 11 - Ultraviolet Quantum Efficiency

Angular Quantum Efficiency

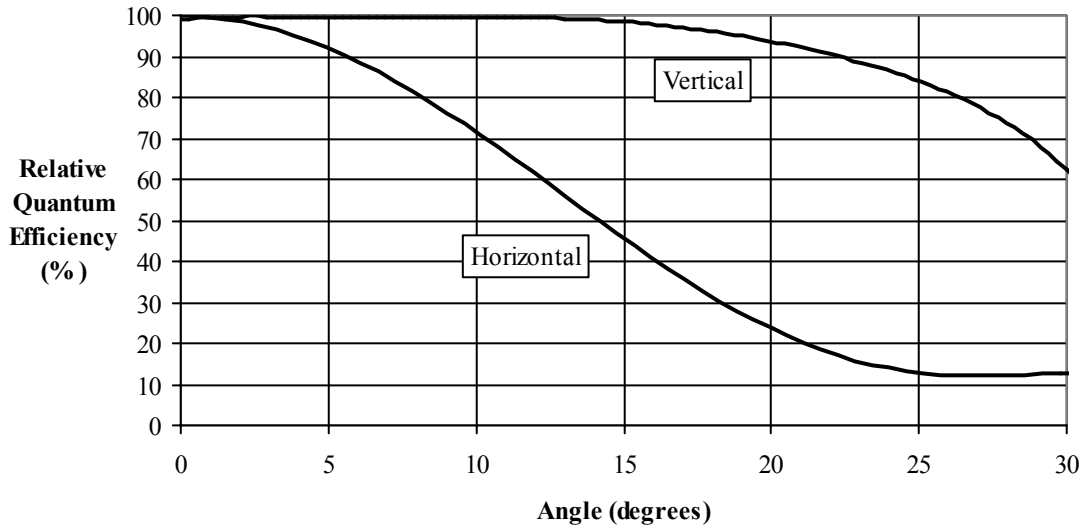


Figure 12 - Angular Quantum Efficiency

Dark Current versus Temperature

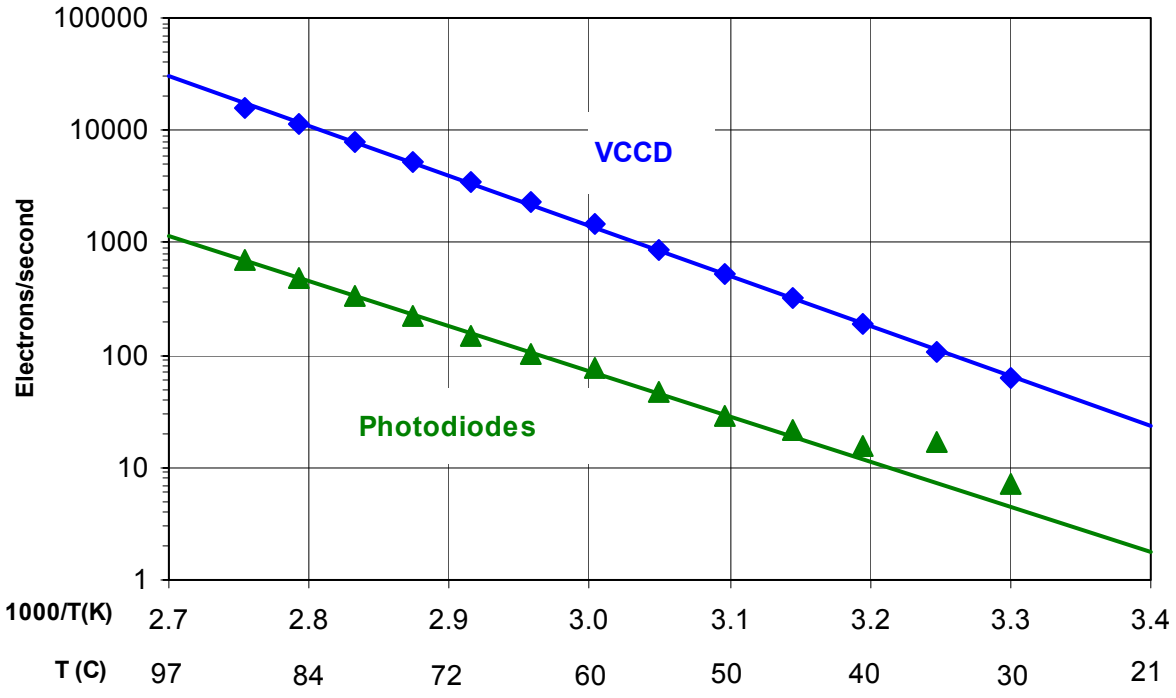


Figure 13 - Dark Current versus Temperature

TEST DEFINITIONS

Test Regions of Interest

Active Area ROI: Pixel 1, 1 to Pixel 1600,1200
Center 100 by 100 ROI: Pixel 750,550 to Pixel 849, 649

Only the active pixels are used for performance and defect tests.

OverClocking

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 14 for a pictorial representation of the regions.

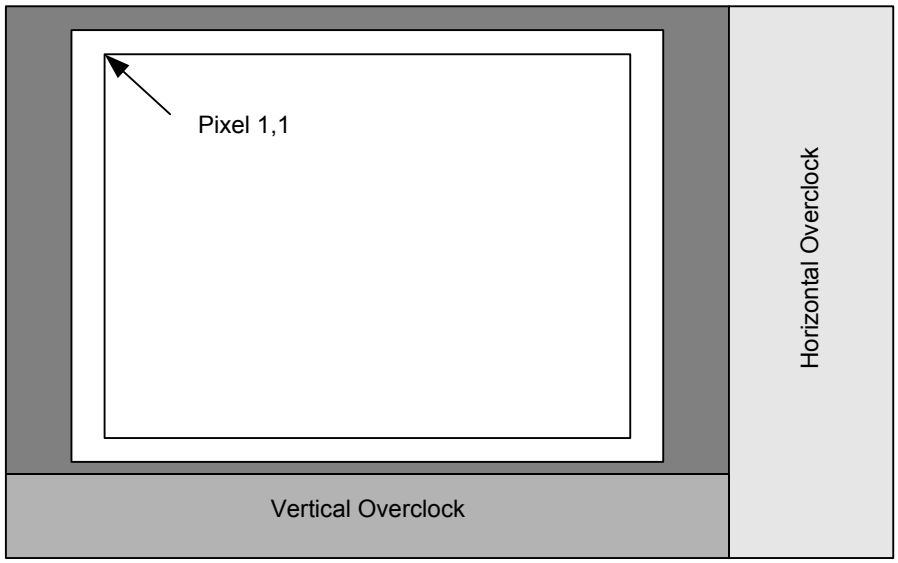


Figure 14 - Overclock Regions of Interest

Tests

1. **Dark Field Center Uniformity**
   This test is performed under dark field conditions. Only the center 100 by 100 pixels of the sensor are used for this test - pixel (750,550) to pixel (849,649).

$$\text{Dark field center uniformity} = \text{Standard Deviation of center 100 by 100 pixels in electrons} * \left(\frac{\text{DPS Integration time}}{\text{Actual integration time used}} \right)$$

   Units: e^- rms
   DPS integration time: Device Performance Specification Integration Time = 33msec

2. **Dark Field Global Uniformity**
   This test is performed under dark field conditions. The sensor is partitioned into 192 sub regions of interest, each of which is 100 by 100 pixels in size. See Figure 15 - Test Sub Regions of Interest. The average signal level of each of the 192 sub regions of interest is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

   Signal of ROI[i] = (ROI Average in ADU – Horizontal overclock average in ADU) * mV per count
   Where i = 1 to 192. During this calculation on the 192 sub regions of interest, the maximum and minimum signal levels are found.

   The dark field global uniformity is then calculated as the maximum signal found minus the minimum signal level found.

   Units: mVpp (millivolts peak to peak)

3. **Global Uniformity**
   This test is performed with the imager illuminated to a level such that the output is at 80% of saturation (approximately 32,000 electrons). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 40,000 electrons. Global uniformity is defined as

$$\text{Global Uniformity} = 100 * \left(\frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}} \right)$$

   Units: %rms
   Active Area Signal = Active Area Average – Horizontal Overclock Average

4. Global Peak to Peak Uniformity

This test is performed with the imager illuminated to a level such that the output is at 80% of saturation (approximately 32,000 electrons). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 40,000 electrons. The sensor is partitioned into 192 sub regions of interest, each of which is 100 by 100 pixels in size. See Figure 15 - Test Sub Regions of Interest. The average signal level of each of the 192 sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

Signal of ROI[i] = (ROI Average in ADU – Horizontal overclock average in ADU) * mV per count
Where i = 1 to 192. During this calculation on the 192 sub regions of interest, the maximum and minimum signal levels are found.

The global peak to peak uniformity is then calculated as:

$$\text{Global Uniformity} = \frac{\text{Maximum Signal - Minimum Signal}}{\text{Active Area Signal}}$$

Units: %pp

5. **Center Uniformity**

This test is performed with the imager illuminated to a level such that the output is at 80% of saturation (approximately 32,000 electrons). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 40,000 electrons. Defects are excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels (See Figure 15 - Test Sub Regions of Interest) of the sensor. Center uniformity is defined as:

$$\text{Center ROI Uniformity} = 100 * \left(\frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}} \right)$$

Units: %rms
Center ROI Signal = Center ROI Average – Horizontal Overclock Average

6. Dark field defect test

This test is performed under dark field conditions. The sensor is partitioned into 192 sub regions of interest, each of which is 100 by 100 pixels in size. See Figure 15 - Test Sub Regions of Interest. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in “Defect Definitions” section.

7. Bright field defect test

This test is performed with the imager illuminated to a level such that the output is at 80% of saturation (approximately 32,000 electrons). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 40,000 electrons. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark defect threshold = Active Area Signal * threshold
Bright defect threshold = Active Area Signal * threshold

The sensor is then partitioned into 192 sub regions of interest, each of which is 100 by 100 pixels in size. See Figure 15 - Test Sub Regions of Interest. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 416 mV (32,000 electrons).
- Dark defect threshold: 416mV * 15% = 62.4 mV
- Bright defect threshold: 416mV * 15% = 62.4 mV
- Region of interest #1 selected. This region of interest is pixels 1,1 to pixels 100,100.
  - Median of this region of interest is found to be 416 mV.
  - Any pixel in this region of interest that is >= (416+62.4 mV) 478.4 mV in intensity will be marked defective.
  - Any pixel in this region of interest that is <= (416-62.4 mV) 353.6 mV in intensity will be marked defective.
- All remaining 191 sub regions of interest are analyzed for defective pixels in the same manner.

Test Sub Regions of Interest

Pixel (1,1)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96
97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112
113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128
129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144
145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160
161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176
177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192

Pixel (1600,1200)

Figure 15 - Test Sub Regions of Interest

OPERATION

Maximum Ratings

Description	Symbol	Minimum	Maximum	Units	Notes
Temperature	T	-50	70	°C	1
Humidity	RH	5	90	%	2
Output Bias Current	Iout	0.0	10.0	mA	3
Off-chip Load	C_L		10	pF	4

Notes:
1. Noise performance will degrade at higher temperatures.
2. T=25ºC. Excessive humidity will degrade MTTF.
3. Total for both outputs. Current is 5 mA for each output. Note that the current bias affects the amplifier bandwidth.
4. With total output load capacitance of CL = 10pF between the outputs and AC ground.
5. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged.

Caution: This device contains limited protection against Electrostatic Discharge (ESD)
Devices should be handled in accordance with strict ESD procedures for Class 0 devices (JESD22 Human Body Model) or Class A (Machine Model). Refer to Application Note MTD/PS-0224, "Electrostatic Discharge Control"

Caution: Improper cleaning of the cover glass may damage these devices.
Refer to Application Note MTD/PS-0237, "Cover Glass Cleaning for Image Sensors"

Caution: Each sensor is shipped with a protective tape on the cover glass. Care should be used when removing the tape to prevent ESD damage. The tape should be removed when the sensor is in the shipping container or when the sensor in a camera.

DC Bias Operating Conditions

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Output Gate	OG	-3.0	-2.5	-2.0	V	1 µA	
Reset Drain	RD	11.5	12.0	12.5	V	1 µA	
Output Amplifier Supply	VDD	14.5	15.0	15.5	V	1 mA	1
Ground	GND	0.0	0.0	0.0	V		
Substrate	SUB	8.0	Vab	17.0	V		2
ESD Protection	ESD	-8.0	-7.0	-6.0	V		3
Output Amplifier Return	VSS	0.0	0.7	1.0	V		

Notes:
1. The operating value of the substrate voltage, Vab, will be marked on the shipping container for each device. The value Vab is set such that the photodiode charge capacity is 40,000 electrons.
2. VESD must be at least 1 Volt more negative than H1L, H2L and RL during sensors operation *AND* during camera power turn on.
3. One output, unloaded

AC Operating Conditions

Clock Levels

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Vertical CCD Clock High	V2H	7.5	8.0	8.5	V	
Vertical CCD Clocks Midlevel	V1M, V2M	-0.2	0.0	0.2	V	
Vertical CCD Clocks Low	V1L, V2L	-9.5	-9.0	-8.5	V	
Horizontal CCD Clocks Amplitude	H1H, H2H	4.5	5.0	5.5	V	
Horizontal CCD Clocks Low	H1L, H2L	-5.0	-4.0	-3.8	V	
Reset Clock Amplitude	RH		5.0		V	1
Reset Clock Low	RL	-4.0	-3.5	-3.0	V	2
Electronic Shutter Voltage	Vshutter	44	48	52	V	
Fast Dump High	FDH	4.8	5.0	5.2	V	
Fast Dump Low	FDL	-9.5	-9	-8	V	

Notes:
1. Reset amplitude must be set to 7.0 V for 80,000 electrons output in summed interlaced or binning modes.
2. Reset low level must be set to –5.0 V for 80,000 electrons output in summed interlaced or binning modes.

Clock Line Capacitances

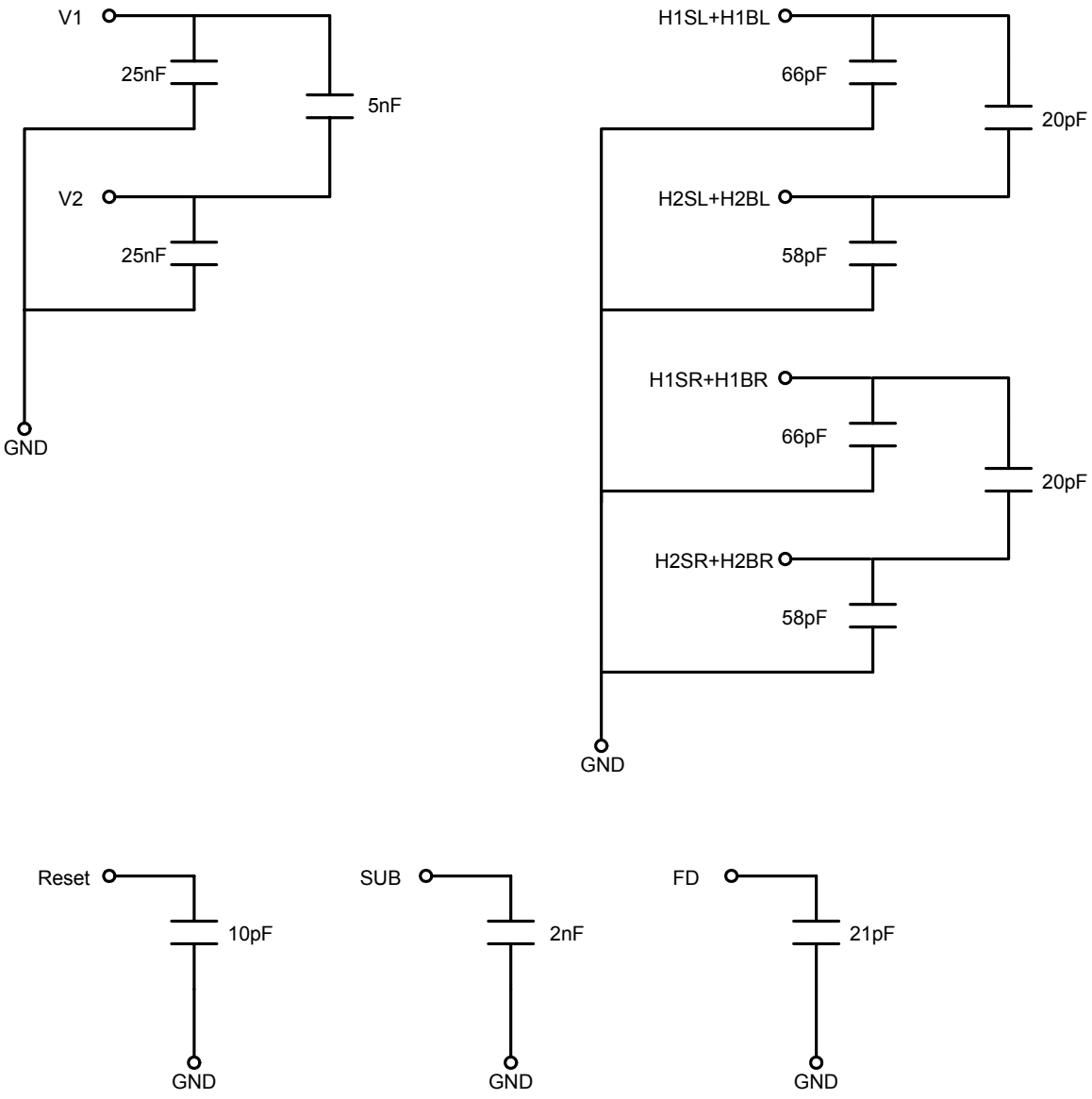


Figure 16 - Clock Line Capacitances

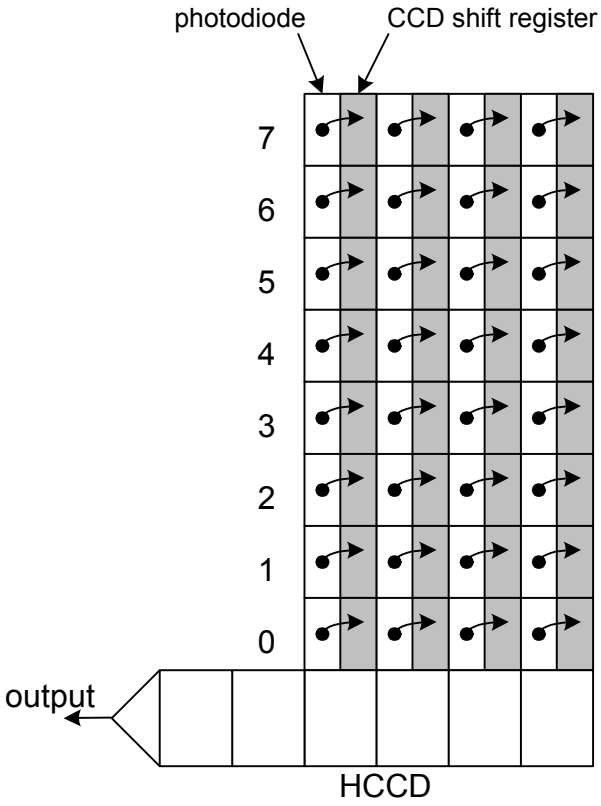
Timing Requirements

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
HCCD Delay	T_{HD}	1.3	1.5	10.0	µs	
VCCD Transfer time	T_{VCCD}	1.3	1.5	20.0	µs	
Photodiode Transfer time	T_{V3rd}	8.0	12.0	15.0	µs	
VCCD Pedestal time	T_{3P}	20.0	25.0	50.0	µs	
VCCD Delay	T_{3D}	15.0	20.0	100.0	µs	
Reset Pulse time	T_R	5.0	10.0		ns	
Shutter Pulse time	T_S	3.0	5.0	10.0	µs	
Shutter Pulse delay	T_{SD}	1.0	1.6	10.0	µs	
HCCD Clock Period	T_H	25.0	50.0	200.0	ns	
VCCD rise/fall time	T_{VR}	0.0	0.1	1.0	µs	
Fast Dump Gate delay	T_{FD}	0.0	0.0	0.5	µs	
Vertical Clock Edge Alignment	T_{VE}	0.0		100.0	ns	

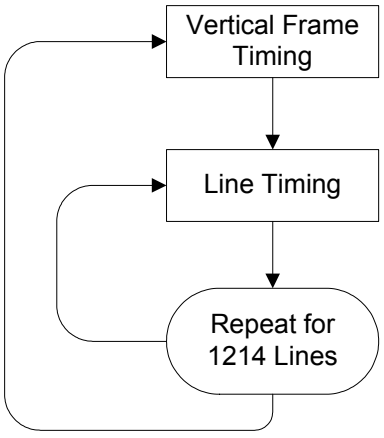
Notes:

Timing Modes

Progressive Scan



In progressive scan read out every pixel in the image sensor is read out simultaneously. Each charge packet is transferred from the photodiode to the neighboring vertical CCD shift register simultaneously. The maximum useful signal output is limited by the photodiode charge capacity to 40,000 electrons.



Frame Timing

Frame Timing without Binning - Progressive Scan

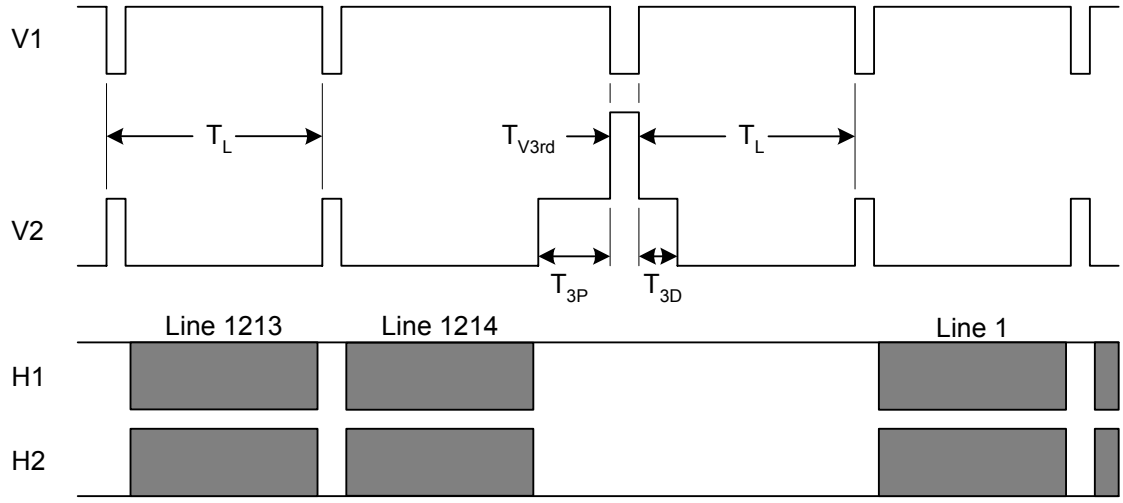


Figure 17 - Framing Timing without Binning

Frame Timing for Vertical Binning by 2 - Progressive Scan

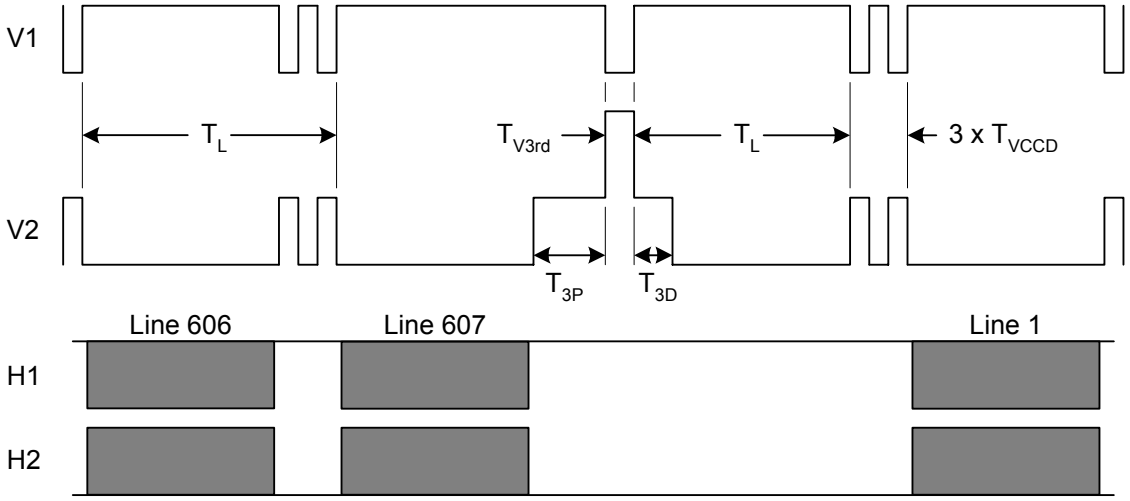


Figure 18 - Frame Timing for Vertical Binning by 2

Frame Timing Edge Alignment

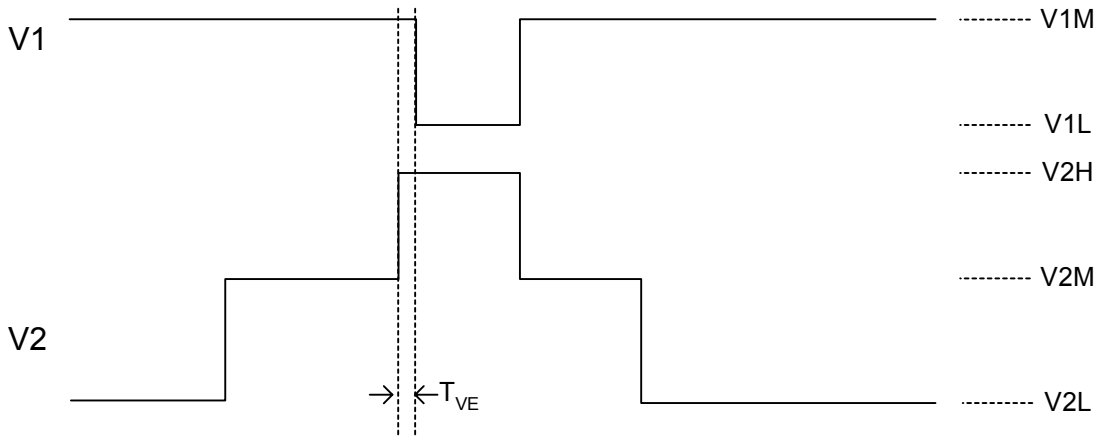


Figure 19 - Frame Timing Edge Alignment

Line Timing

Line Timing Single Output – Progressive Scan

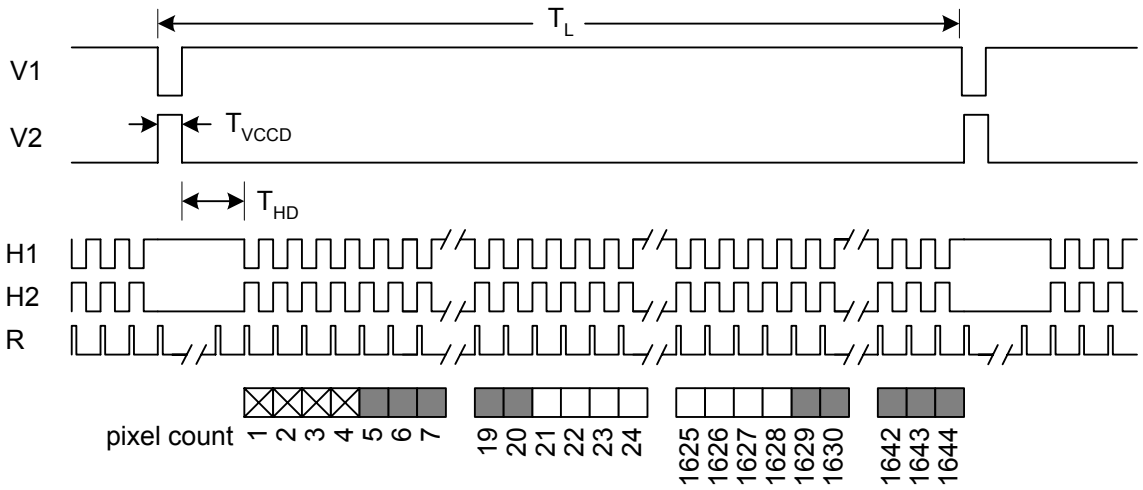


Figure 20 - Line Timing Single Output

Line Timing Dual Output – Progressive Scan

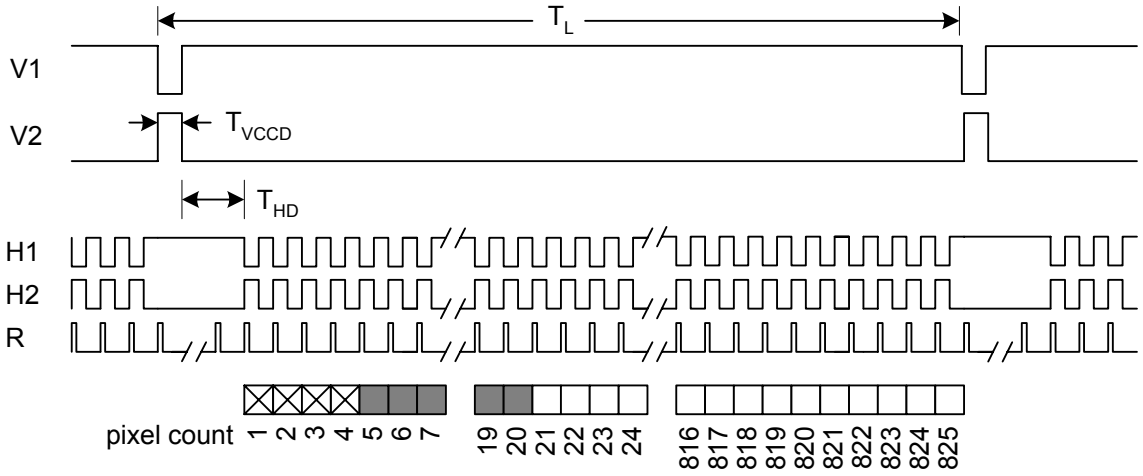


Figure 21 - Line Timing Dual Output

Line Timing Vertical Binning by 2 – Progressive Scan

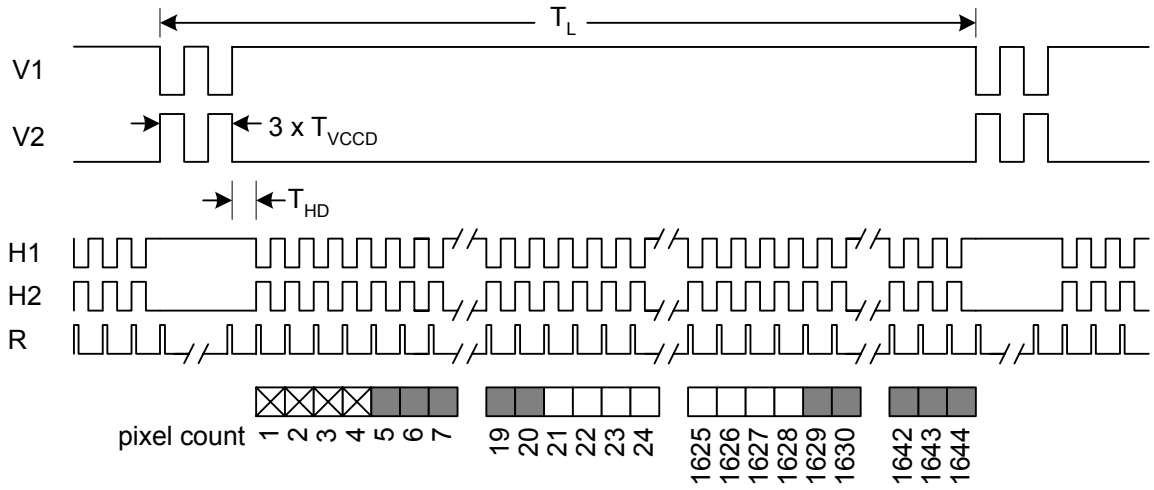


Figure 22 - Line Timing Vertical Binning by 2

Line Timing Detail – Progressive Scan

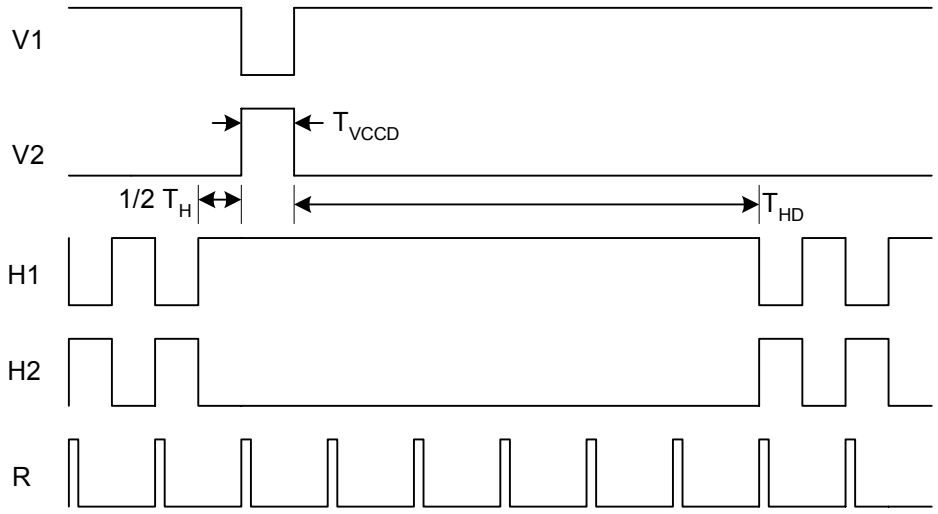


Figure 23 - Line Timing Detail

Line Timing Binning by 2 Detail – Progressive Scan

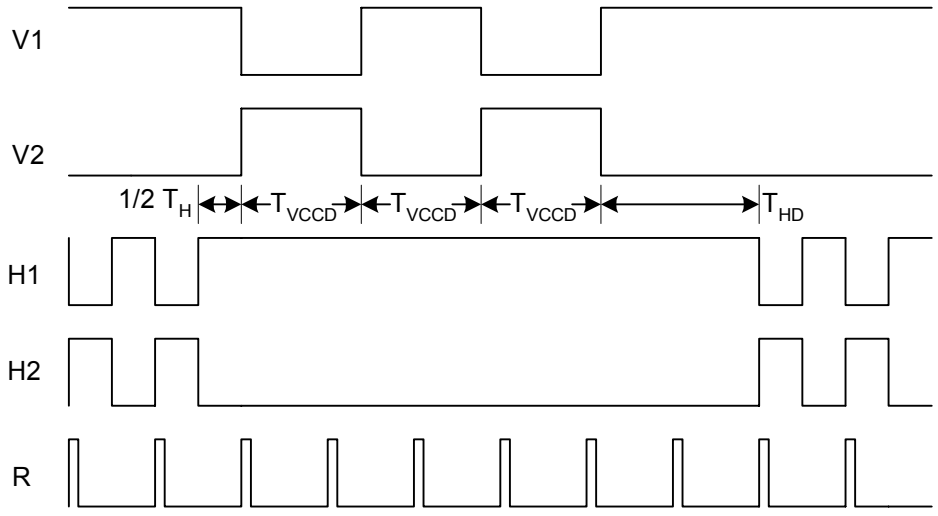


Figure 24 - Line Timing by 2 Detail

Line Timing Edge Alignment

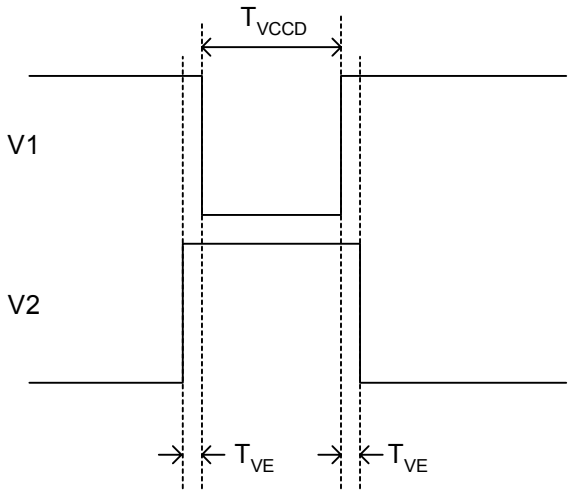


Figure 25 - Line Timing Edge Alignment

Pixel Timing

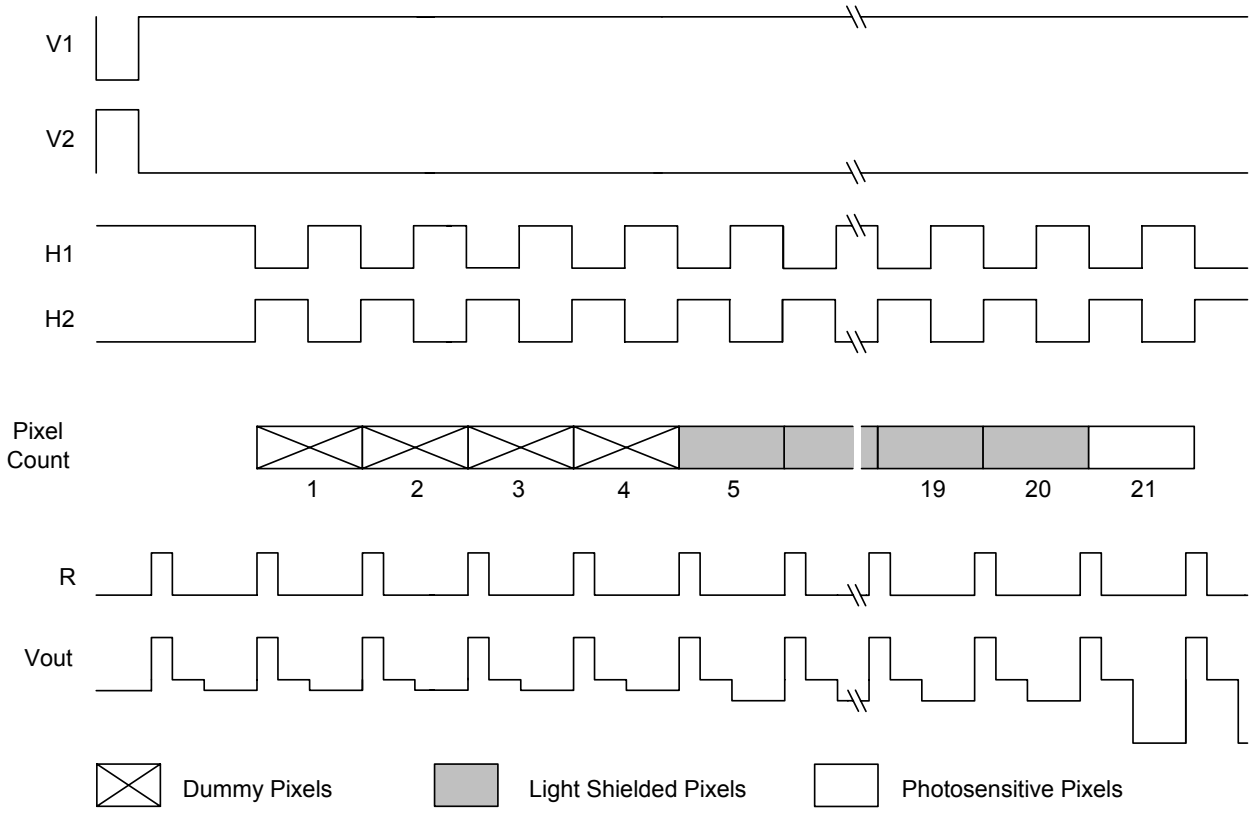


Figure 26 - Pixel Timing

Pixel Timing Detail

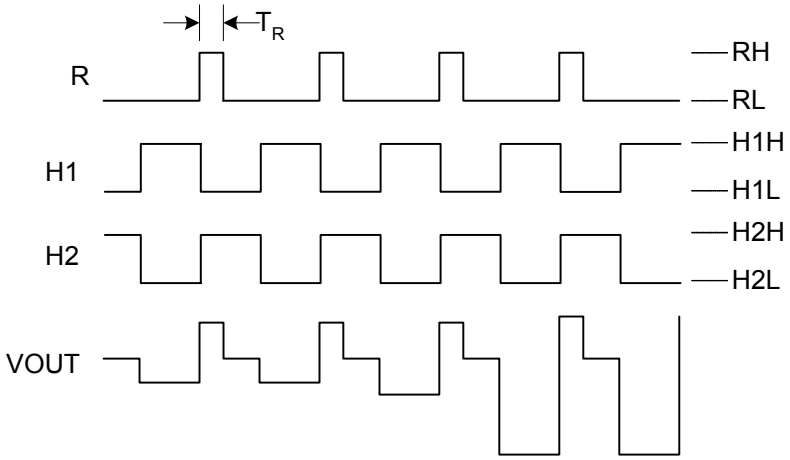


Figure 27 - Pixel Timing Detail

Fast Line Dump Timing

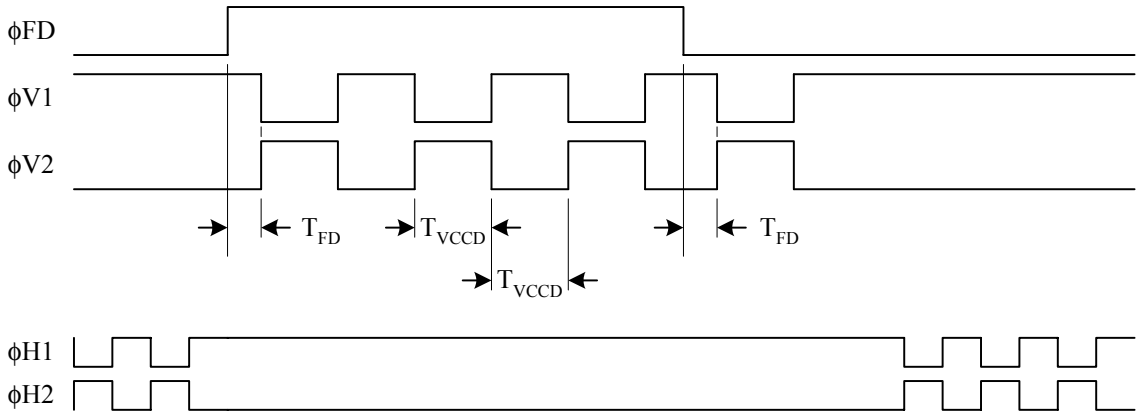


Figure 28 - Fast Line Dump Timing

Electronic Shutter

Electronic Shutter Line Timing

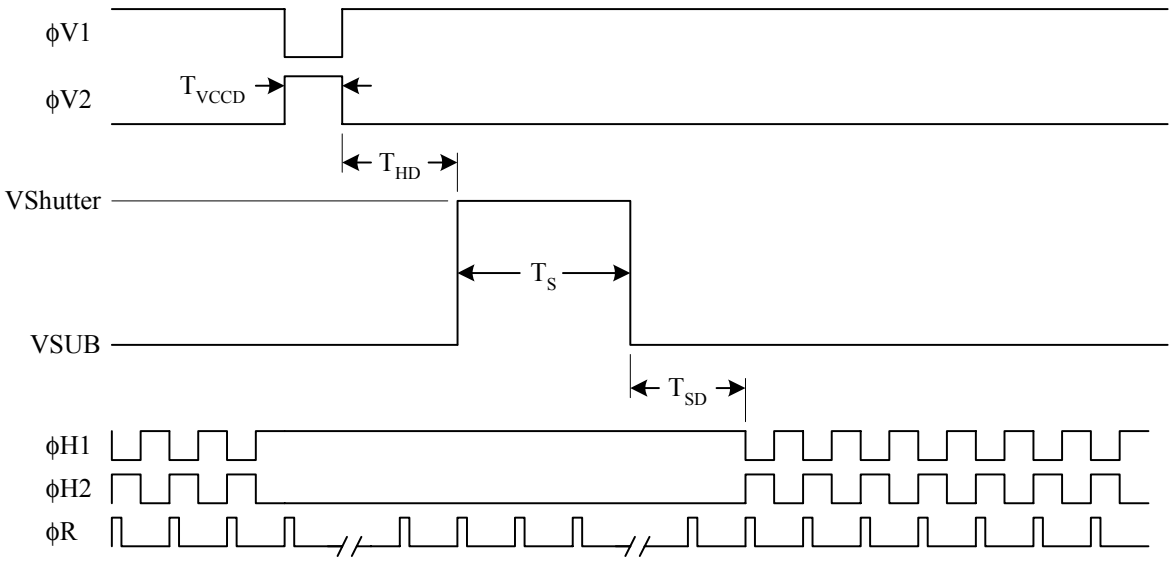


Figure 29 - Electronic Shutter Line Timing

Electronic Shutter – Integration Time Definition

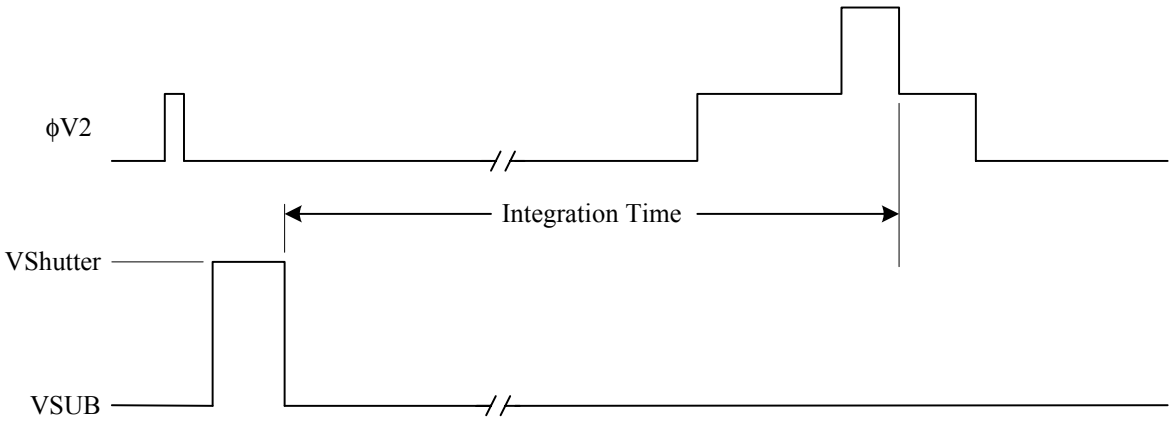


Figure 30 - Integration Time Definition

Electronic Shutter Description

The voltage on the substrate (SUB) determines the charge capacity of the photodiodes. When SUB is 8 volts the photodiodes will be at their maximum charge capacity. Increasing VSUB above 8 volts decreases the charge capacity of the photodiodes until 48 volts when the photodiodes have a charge capacity of zero electrons. Therefore, a short pulse on SUB, with a peak amplitude greater than 48 volts, empties all photodiodes and provides the electronic shuttering action.

It may appear the optimal substrate voltage setting is 8 volts to obtain the maximum charge capacity and dynamic range. While setting VSUB to 8 volts will provide the maximum dynamic range, it will also provide the minimum antiblooming protection.

The KAI-2001 VCCD has a charge capacity of 55,000 electrons (55 ke^-). If the SUB voltage is set such that the photodiode holds more than 55 ke^-, then when the charge is transferred from a full photodiode to VCCD, the VCCD will overflow. This overflow condition manifests itself in the image by making bright spots appear elongated in the vertical direction. The size increase of a bright spot is called blooming when the spot doubles in size. The blooming can be eliminated by increasing the voltage on SUB to lower the charge capacity of the photodiode. This ensures the VCCD charge capacity is greater than the photodiode capacity. There are cases where an extremely bright spot will still cause blooming in the VCCD. Normally, when the photodiode is full, any additional electrons generated by photons will spill out of the photodiode. The excess electrons are drained harmlessly out to the substrate. There is a maximum rate at which the electrons can be drained to the substrate. If that maximum rate is exceeded, (for example, by a very bright light source) then it is possible for the total amount of charge in the photodiode to exceed the VCCD capacity. This results in blooming. The amount of antiblooming protection also decreases when the integration time is decreased. There is a compromise between photodiode dynamic range (controlled by VSUB) and the amount of antiblooming protection. A low VSUB voltage provides the maximum dynamic range and minimum (or no) antiblooming protection. A high VSUB voltage provides lower dynamic range and maximum antiblooming protection. The optimal setting of VSUB is written on the container in which each KAI-2001 is shipped. The given VSUB voltage for each sensor is selected to provide antiblooming protection for bright spots at least 100 times saturation, while maintaining at least 40 ke^- of dynamic range.

The electronic shutter provides a method of precisely controlling the image exposure time without any mechanical components. If an integration time of T_{INT} is desired, then the substrate voltage of the sensor is pulsed to at least 40 volts T_{INT} seconds before the photodiode to VCCD transfer pulse on V2. Use of the electronic shutter does not have to wait until the previously acquired image has been completely read out of the VCCD.

Large Signal Output

When the image sensor is operated in the binned or summed interlaced modes there will be more than 40,000 electrons in the output signal. The image sensor is designed with a 16µV/e charge to voltage conversion on the output. This means a full signal of 40,000 electrons will produce a 640 mV change on the output amplifier. The output amplifier was designed to handle an output swing of 640 mV at a pixel rate of 40 MHz. If 80,000 electron charge packets are generated in the binned or summed interlaced modes then the output amplifier output will have to swing 1280 mV. The output amplifier does not have enough bandwidth (slew rate) to handle 1280 mV at 40 MHz. Hence, the pixel rate will have to be reduced to 20 MHz if the full dynamic range of 80,000 electrons is desired.

The charge handling capacity of the output amplifier is also set by the reset clock voltage levels. The reset clock driver circuit is very simple if an amplitude of 5 V is used. But the 5 V amplitude restricts the output amplifier charge capacity to 40,000 electrons. If the full dynamic range of 80,000 electrons is desired then the reset clock amplitude will have to be increased to 7 V.
If you only want a maximum signal of 40,000 electrons in binned or summed interlaced modes, then a 40 MHz pixel rate with a 5 V reset clock may be used. The output of the amplifier will be unpredictable above 40,000 electrons so be sure to set the maximum input signal level of your analog to digital converter to the equivalent of 40,000 electrons (640 mV).

STORAGE AND HANDLING

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Temperature	T	-55	80	°C	1
Humidity	RH	5	90	%	2

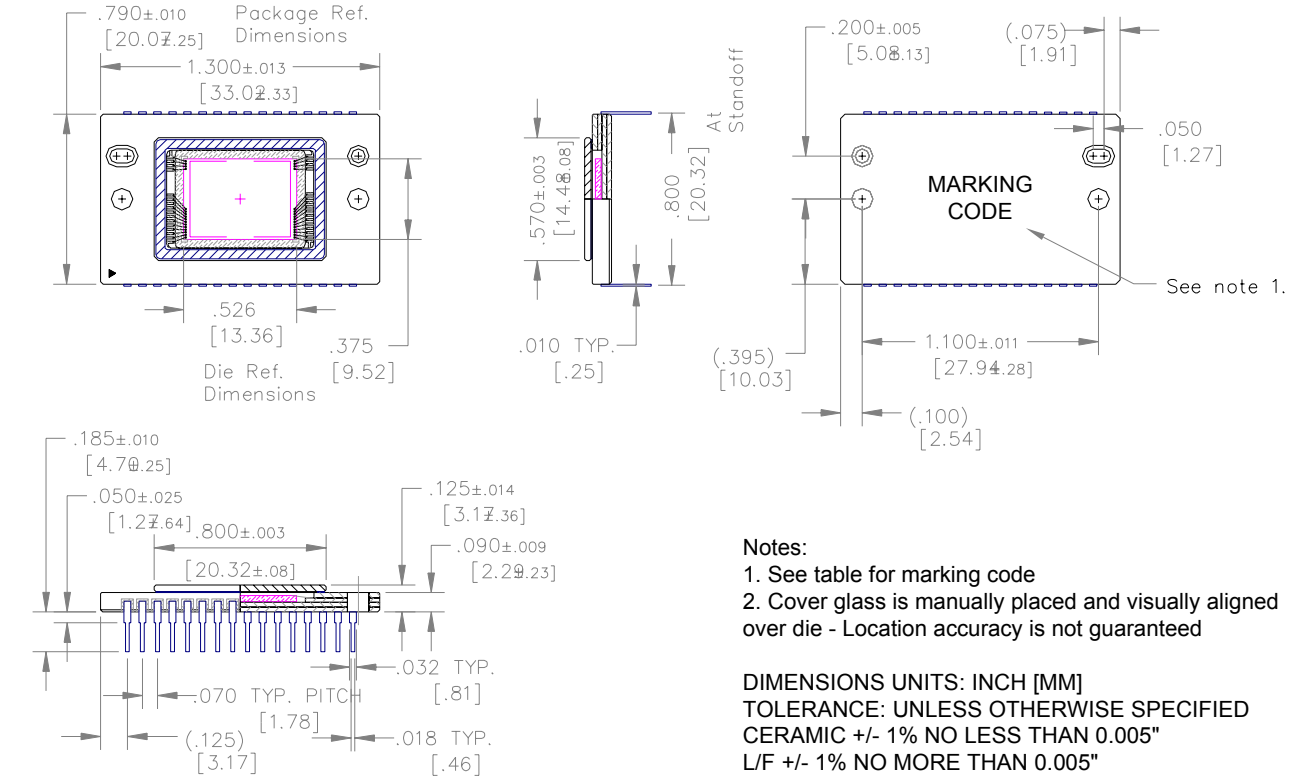
Notes:
1. Long-term exposure toward the maximum temperature will accelerate color filter degradation.
2. T=25ºC. Excessive humidity will degrade MTTF.

Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370ºC. Failure to do so may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating. Kodak recommends the use of a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

MECHANICAL DRAWINGS

Package



Notes:
1. See table for marking code
2. Cover glass is manually placed and visually aligned over die - Location accuracy is not guaranteed

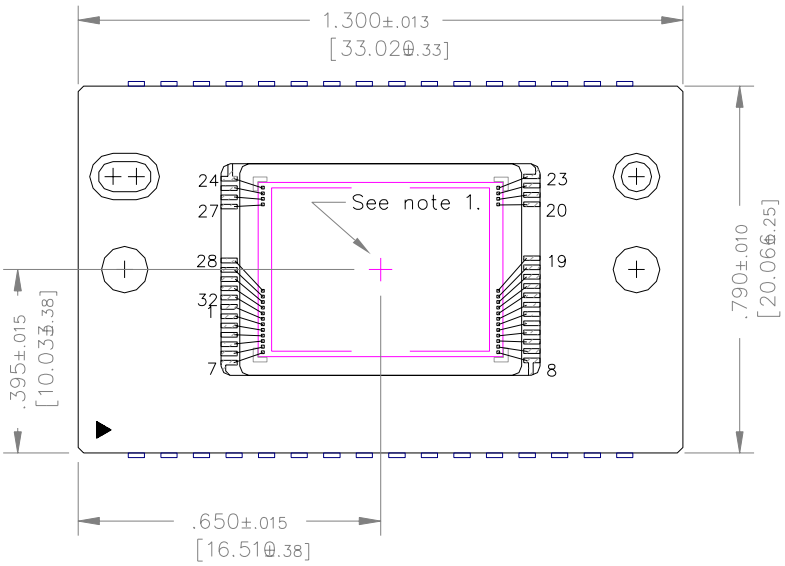
DIMENSIONS UNITS: INCH [MM]
TOLERANCE: UNLESS OTHERWISE SPECIFIED
CERAMIC +/- 1% NO LESS THAN 0.005"
L/F +/- 1% NO MORE THAN 0.005"

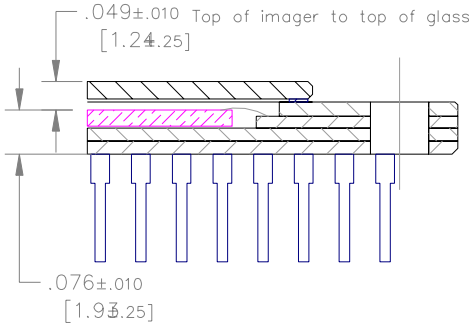
Figure 31 - Package Drawing

Note 1:

Configuration	Marking Code
Monochrome	KAI-2001 SN
Monochrome with Lenslets	KAI-2001M SN
Color with Lenslets	KAI-2001CM SN

Die to Package Alignment



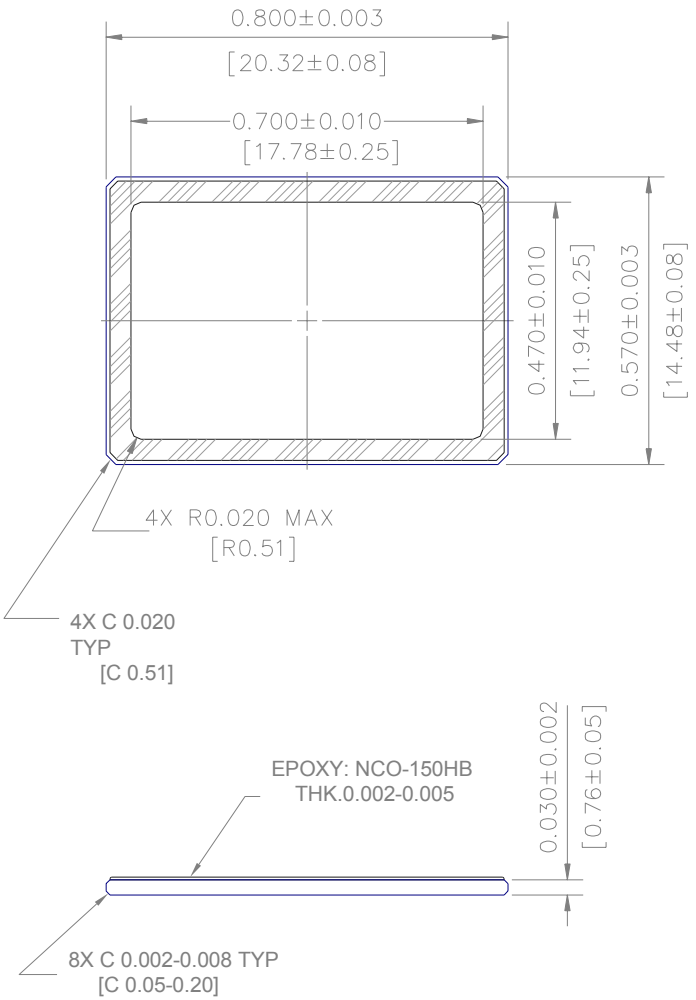


Notes:
1. Center of image is offset from center of package by (0.00, 0.00) mm nominal.
2. Die is aligned within +/- 2 degree of any package cavity edge.

DIMENSIONS UNITS: IN [MM]
TOLERANCES: UNLESS OTHERWISE SPECIFIED
CERAMIC +/- 1% NO LESS THAN 0.005"
L/F +/- 1% NO MORE THAN 0.005"

Figure 32 - Die to Package Alignment

Glass



NOTES:
1. MATERIALS: SUBSTRATE = SCHOTT D-263
EPOXY = NCO-150HB
THK = 0.002 - 0.005
2. DUST/SCRATCH COUNT = 10 MICRON MAX
3. DOUBLE SIDED AR COATING REFLECTANCE:
420 - 435 nm < 2.0%
435 - 630 nm < 0.8%
630 - 680 nm < 2.0%

UNITS: IN [MM]
TOLERANCE: UNLESS OTHERWISE SPECIFIED
+/- 1% NO LESS THAN 0.005"

Figure 33 - Glass Drawing

Glass Transmission

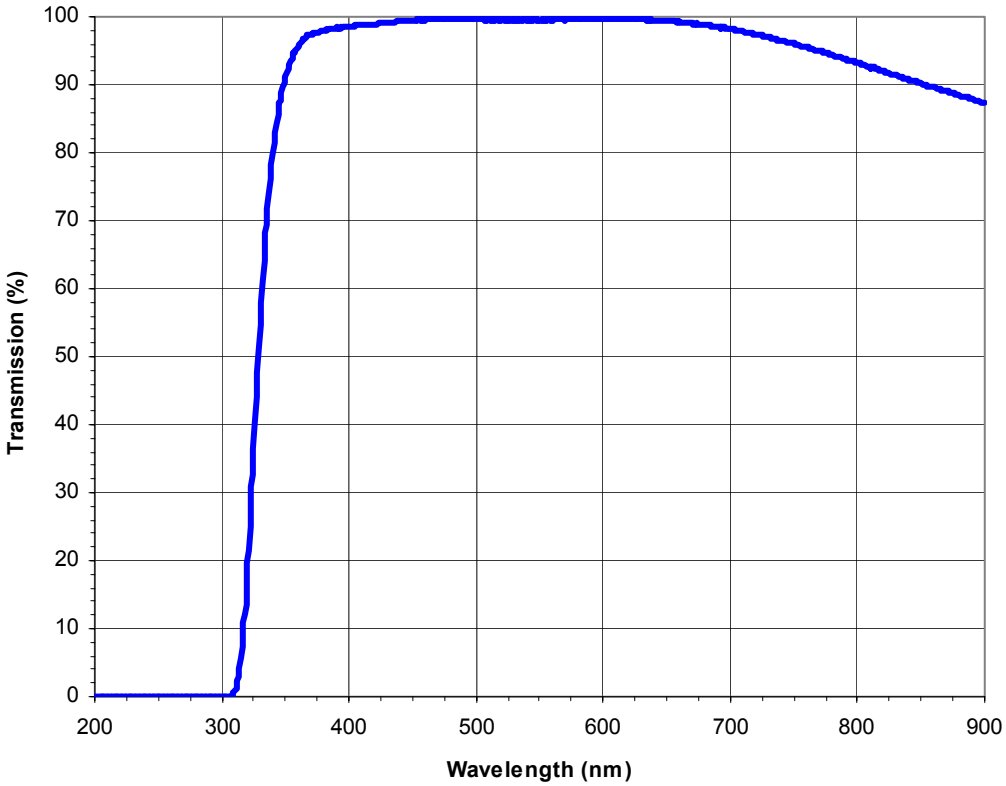


Figure 34 - Glass Transmission

QUALITY ASSURANCE AND RELIABILITY

Quality Strategy: All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

Liability of the Supplier: A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

Liability of the Customer: Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Cleanliness: Devices are shipped free of mobile contamination inside the package cavity. Immovable particles and scratches that are within the imager pixel area and the corresponding cover glass region directly above the pixel sites are also not allowed. The cover glass is highly susceptible to particles and other contamination. Touching the cover glass must be avoided. See ISS Application Note MTD/PS-0237, Cover Glass Cleaning for Image Sensors, for further information.

ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe workstations. See ISS Application Note MTD/PS-0224, Electrostatic Discharge Control, for handling recommendations.

Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Test Data Retention: Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical: The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

ORDERING INFORMATION

Available Part Configurations

Type	Description	Glass Configuration
KAI-2001	Monochrome without microlens	Taped Clear Glass or Sealed Quartz Glass
KAI-2001M	Monochrome with microlens	Sealed MAR Glass
KAI-2001CM	Color with microlens	Sealed MAR Glass

Please contact Image Sensor Solutions for available part numbers.
MAR Glass: Anti-reflective coating, both sides of glass.

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
1.0	Initial formal version